Amendments to the Specification:

Please amend the specification as follows:

Please replace the title of the invention with "A MOSFET WITH A THIN GATE INSULATING FILM".

On page 1, before the heading (BACKGROUND OF THE INVENTION) insert the following:

CORRESPONDING RELATED APPLICATIONS

This application is a continuation of Application Serial No. 10/160,036 filed June 4, 2002, which is a continuation of Application Serial No. 09/828,205 filed on April 9, 2001; which is a continuation of 09/440,938 filed November 6, 1999; which in turn is a continuation of 08/527,562 filed September 13, 1995.

Please replace the first full paragraph on page 2 with the following rewritten paragraph:

To overcome this problem, in 1993, Fiegna et al. have proposed such a technique that although the gate insulating film thickness is fixed to about 3 nm, the composing elements other than the gate insulating film can be reduced [[[]](as reported by Document (Writer): C. Fiegna. H. Iwai, T. Wada, T. Saito, E. Sangiorgio, and B. Ricco; (Title) a new scaling methodology for the 0.1 to 0.021 um MOSFET, 'Dig. of Tech. Papers, VLSI Symp; (Source) Technol., Kyoto, pp. 33-34, 1993). On the basis of this technique, in the same year, Ono et al. have realized a translator having a gate length of 0.04 um, [as reported by Document (Writer): M. Ono, M. Saito, T. Yoshitomi, C. Fiegna, and H. Iwai; (Title) Sub-50 nm gate length n-MOSFETs with 10 nm phosphorus source and drain junction: (Source) IEDM Tech. Dig., pp. 119 to 122, 1993)[[]]].

Please replace the second full paragraph on page 7 with the following rewritten paragraph:

Fig. 13A is a graphical representation[[s]] showing the dependence of the drain current I_d characteristics upon the drain voltage V_d in the prior art transistor with the gate voltage V_g as a parameter;

Please replace the fourth full paragraph on page 7 with the following rewritten paragraph:

Fig. 14A is a graphical representation[[s]] showing the dependence of the transconductance gm upon the gate voltage V_g in the prior art transistor;

Please replace the tenth full paragraph on page 7 with the following rewritten paragraph:

Fig. 18A is an illustration showing an example of the semiconductor device, in which the whole area of the semiconductor device ~~are~~ **is** formed by the transistors according to the present invention;

Please replace the fourth full paragraph on page 9 with the follow rewritten paragraph

Fig. 27B is ~~the similar~~ a more detailed graphical representation showing the $(I_g - V_g)$ characteristics of the gate insulating films of various film thicknesses t_{ox} used for the ordinary tunneling gate oxide film MOSFET, in which the film thicknesses are more limited;

Please replace the sixth full paragraph on page 9 with the following rewritten paragraph:

Fig. 28B is a circuit diagram showing ~~to~~ the structure of the MOSFET having a Schtokky diode to protect the gate insulating film of the transistor according to the present invention;

Please replace the third full paragraph on page 12 with the following rewritten paragraph:

Fig. 3 shows the ~~dependance~~ dependence of the transconductance (gm) degradation rate (%) upon the gate oxide film thickness (T_{ox}) under hot carrier stress (stress condition V_d-

2.5V; I_{submax}). Fig. 3 indicates that when the gate oxide film thickness is less than 2.5 nm, the degradation rate of the transconductance gm can be reduced down to about half of the degradation rate obtained when the gate oxide film thickness is 3 nm (this thickness has been so far considered as a limit value at which tunneling current begins to flow), and thereby the life time of the transistor can be increased ~~twice~~ two times or more. Therefore, it is desirable that the gate oxide film thickness T_{ox} is determined less than 2.5 nm.

Please replace the first full paragraph on page 18 with the following rewritten paragraph:

Figs. 15A and 15B show the transistor characteristics when the supply voltage V_d is 0.5 V or less. In this case, the gate voltage V_g is also 0.5 V or less. In this case, the gate voltage V_g is also 0.5 V or less. In these drawings, the major characteristics are shown in comparison between the invention transistor (Fig. 15A) and the prior art transistor (Fig. 15D). Here, the major characteristics are the current drive capability (I_d - V_d) characteristics; sub-threshold characteristics, the (log I_d - V_g) characteristics, and the transconductance (gm - V_g) characteristics. These drawings indicate that in the case of the invention transistor, a larger drain current I_d and a large transconductance gm can be both obtained at a lower supply voltage, as compared with the prior art transistor, so that the overall characteristics of the invention transistor can be improved. For instance, in the invention transistor, in ~~spit~~ spite of such a low supply voltage as 0.5 V, an excellent transconductance gm as high as 746 mS/mm can be obtained.

Please replace the first full paragraph on page 23 with the following rewritten paragraph:

~~Alphabets in circles~~ Letters in circles denote improvements of operation performances. Condition b (1.3V operation) of transistor C shows that power consumption is the same and frequency becomes 5.5 times of those of condition a of the transistor A. In condition c (1.2V operation), power consumption is the same and frequency becomes 7.8 times. In condition d (0.3V operation) power consumption becomes 1/100 at the same frequency. In condition e (0.5V operation), power consumption becomes 1/20 while operation frequency is increased to

2.1 times. In condition f (0.5V operation), power consumption becomes 1/9 while operation frequency is increased to five times.

Please replace the fourth full paragraph on page 24 (bridging to page 25), with the following rewritten paragraph:

Further, in the case of the ordinary transistors, the transconductance gm so far obtained at the supply voltage of 1.8 V is 480 mS/mm or less in the nMOS of a channel length of 0.05 μm (the gate length is presumed to be 0.10 μm), and 250 mS/mm or less in the pMOS of a channel length of 0.06 μm (the gate length is presumed to be 0.14 μm), [[[]](for instance, as reported by Document ((Writer): G. G. Shahidi, J. Warnock, A. Acovic, P. Agnello, C. Blair, C. Bucelot, A. Burghartz, E. Crabbe, J. Cressler, P. Coane, J. Comfort, B. Davarl, S. Fischer, E. Ganin, S. Gittleman, J. Keller, K. Jenkins, D. Klans, K. Kiewtniak, T. Lu, P. A. McFarland, T. Ning, M. Polcari, S. Subbana, J. Y. Sun, D. Sunderland, A.C. Warren, C. Wong; (Title) A HIGH PERFORMANCE 0.15 μm CMOS; (Source) Dig. Of Tech. Paper, VLSI Symp. On Tech. Kyoto. pp. 93-94, 1993 (referred to as a document [[[]](A)[[]]], hereinafter))[[]]].

Please replace the fifth full paragraph on page 30 (bridging to page 31), with the following rewritten paragraph:

In the above description, the transistor according to the present invention has been explained by using a silicon oxide film as the gate insulating film. In the present invention, however, the same effect as described above can be obtained, as far as an insulating film having a gate capacitance equivalent thereto is used. That is, as the insulating film, various films can be used, for instance as follows: silicon nitride film (Si_3N_4), silicon nitric oxide film (SiO_xN_y), a stacked ~~films~~ film of silicon nitride film and silicon oxide film (SiO_2/Si_3N_4, Si_3N_4/SiO_2, $SiO_2/Si_3N_4/SiO_2$, $Si_3N_4/SiO_2/N_4$), a laminated layer of tantalum oxide (TaO_x), titanium oxide strontium ($TiSr_xO_y$) and its silicon oxide film or silicon nitride film, etc. As far as the gate capacitance of these insulating films is equivalent to the silicon oxide film having a film thickness less than 2.5 nm (at the conversion rate to silicon oxide film), the effect of the present invention can be obtained. For instance, since the dielectric constant of silicon nitride film is 7.9 (about twice larger than that (3.9) of silicon oxide film), when the silicon nitride film is used, the same effect as the present invention can be obtained when the film thickness is less than 5 nm. When any of the above-mentioned insulating films is used, even if tunneling leakage current flows through the gate insulating film, this coincides with the ~~gist~~ techniques of the present invention such that the transistor is constructed in such a way that the insulating film thickness is so determined that the tunneling current flows through the silicon oxide film, with the result that the same effect can be obtained. Further, as far as the insulating film having the gate capacitance equivalent to the silicon oxide film whose thickness is less than 2.5 nm is used, an insulating film through which no tunneling current flows can be used. In this case, the power consumption can be reduced, and thereby it is possible to realize a high-performance transistor of lower power consumption.

Please replace the third full paragraph on page 35 with the following rewritten paragraph:

T_{ox} (nm) = ~~long~~ log L_g (μm) + 2.02

Please replace the fifth full paragraph on page 35 with the following rewritten paragraph:

[[$L_g \leq 10\ (T_{ox}\text{-}2.02)$]] $L_g \leq 10^{(T_{OX}\ -\ 2.02)}$.

Please replace the first full paragraph on page 36 with the following rewritten paragraph:

T_{ox} (nm) = ~~long~~ log L_g (μm) + 2.32.

Please replace the third full paragraph on page 36 with the following rewritten paragraph:

[[$L_g \leq 10^{(}T_{ox}{}^{-}2.32^{)}$]] $L_g \leq 10^{(T_{ox}-2.32)}$

it is possible to further improve the performance of the transistor and thereby to apply the transistors to a higher performance LSI.

Please replace the last paragraph on page 36 (bridging to page 37) with the following rewritten paragraph:

Fig. 30A shows MOSFETs 12 according to the present invention, and Fig. 30B shows a conventional MOSFET 13 in comparison with Fig. ~~31A~~ 30A. The MOSFETs 12 shown in Fig. 30A have a performance equivalent to that of the MOSFET 13 shown in Fig. 30B. However, when an appropriate number of the MOSFETS 12 of a short gate length are connected in series, it is possible to realize the circuit having a desired current drive capability, in spite of a small power consumption. In other words, by use of the transistors according to the present invention, it is possible to realize a semiconductor device which can suppress the leakage current sufficiently, that is, which is suitable for a low power consumption.